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CHRISTENSEN, O'CONNOR, JOHNSON, KINDNESS, PLLC
1420 FIFTH AVENUE
SUITE 2800
SEATTLE, WA 98101-2347

EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,977	MOK ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-10 and 14-17* is/are rejected.

7)☒ Claim(s) *2 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed October 05, 205. Claims 11-13 were canceled. Claims 1-10,14-17 are pending, in which claims 14-17 have been newly added.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 1,4,5,7,9,15 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art (present specification page 1, line 20 through page 10; Figs 1-4).

Re claim 1, Applicant's admitted prior art teaches (at present specification page 1, line 20 through page 10; Figs 1-4) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes 104 through a copper stack plate 102/103 (Figs 1a-1b; present specification page 4, lines 10-25); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper (Fig 1c; page 5, lines 1-20); and (c) forming circuit patterns 105 on the copper stack plate (Fig 1d; page 5, line 21 through page 6); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes 204 through a flat-type insulating material provided with release films 202 attached to surfaces of the flat-type insulating material 203 (Figs 2a-2b,3; page 6, line 8 through page 7); (b) filling the via holes with a conductive paste 205 (Fig 2c); and (c) removing the release films 202 from the flat-type insulating material (Fig 2d); (C) alternately arranging the circuit layers and the insulating layers at predetermined positions (Fig 3); (D) pressing the arranged circuit and insulating layers (Fig 4; pages 8-9); wherein circuit patterns from the plated copper 105 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 4,1d; page 5, line 21 through page 6). Re claims 4-5, further comprising the step of: (F) forming a target hole at the position of a target guide mark, serving as a reference point of drilling, on the circuit layers and the insulating layers (re claim 4); and, re claim 5) wherein the sub-step (a) of each of the steps (A) and (B) includes the step of: (a') forming a guide hole at the same position, serving as a reference point of interlayer matching, on the circuit layers and the insulating layers (present specification page 8, line18 through page 9, line 11). Re claim 7, wherein the release

film has a thickness of 20 to 30 microns (specification page 7, lines 1-5). Re claim 9, wherein the conductive paste 205 is considered as a point contact-type conductive paste 205 comprising metal particles (Fig 2c; specification page 7, lines 18-21). Re further claims 15, as similarly applied to claim 1 above, Applicant's admitted prior art also teaches (page 5, lines 1-25) plating surfaces of the copper stack plate and inner walls of the via holes with copper without completely filling the via holes, since the present specification, at page 5, lines 15-20, teaches that "the via holes 104 may be filled with a conductive paste after the inner walls of the via holes 104 are plated". Thereafter, as shown in Figures 3-4, such circuit layers and the insulating layers are arranged and pressed in order to form a parallel multi-layer printed circuit board, wherein circuit patterns from the plated copper are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers.

2. Claims 1,3-5,7-10,14-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al (2004/0194303).

Re claim 1, Kim teaches (at Figs 3A-8; paragraphs 65 through 96) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes 304 through a copper stack plate 302/303 (Figs 3A-3B); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper 305 (Fig 1C); and (c) forming circuit patterns 306 on the copper stack plate (Fig 1d; paragraph 72; 306a-306c in Fig 7); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes 504 through a flat-type insulating material provided with release films 502 attached to surfaces of the flat-type insulating material 503 (Figs 5A-5B); (b) filling the via holes with a conductive paste 505 (Fig 5C); and (c) removing the release films 502 the flat-type insulating material (Fig 5D; paragraphs 81-85); (C) alternately arranging the circuit layers and the insulating layers at predetermined positions (Fig 7, paragraphs 93-97); (D) pressing the arranged circuit and insulating layers (Fig 8), wherein circuit patterns 306a-306c from the plated copper 305 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 7,8, 3d). Re claim 3, wherein surface-treatment of the copper stack plate 105 is performed so as to increase an adhering force (paragraphs 16, 21,24; Figs 1A-1E). Re claims 4-5, further

comprising the step of: (F) forming a target hole at the position of a target guide mark, serving as a reference point of drilling, on the circuit layers and the insulating layers (re claim 4); and, re claim 5) wherein the sub-step (a) of each of the steps (A) and (B) includes the step of: (a') forming a guide hole at the same position, serving as a reference point of interlayer matching, on the circuit layers and the insulating layers (paragraphs 95-96; page 7, right column, lines 7-18). Re claim 7, wherein the release film 502 a thickness of 20 to 30 microns (paragraph 82; Figs 5A-5B). Re claims 8-9, wherein the conductive paste is a metallic bond-type conductive paste 106/505 impregnated with a tin (Sn) component, or re claim 9, wherein the conductive paste is considered as a point contact-type conductive paste 106/505 (paragraphs 16,84). Re claim 10, wherein the flat-type insulating material includes a resin material in a c-stage, and resin layers in a b-stage respectively stacked on both surfaces of the resin material (paragraph 87; Figs 6A-6D,5A-5D). Re further claims 14,16,17, as similarly applied to claim 1 above, Kim also alternatively teaches (at paragraph 61; Figs 2D-2E) about omitting the plugging process of the via holes 204 using the paste 206. Thus, by omitting or not fill the via holes 204 with plating or conductive paste 206 before pressing at Figs 7-8 (paragraphs 61-63,55-60), the via holes are therefore emptied. Thereafter, pressing the arranged circuit layers with the emptied via holes and the insulating layers having conductive paste would fill the emptied via holes in the circuit layers are filled with conductive paste from the insulating layers to electrically connect the insulating layers with the circuit layers. Re further claims 15, as similarly applied to claim 1 above, Kim also alternatively teaches (at paragraphs 60-61; Figs 2C-2E) about plating inner walls of the via holes with copper 205 without completely filling the via holes. Thereafter, as shown in Figure 7-8, arranging and pressing such circuit layers and the insulating layers are arranged and pressed to form a parallel multi-layer printed circuit board, wherein circuit patterns 306a-306c from the plated copper 305 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 7,8, 3d).

Allowable Subject Matter

** As already of record, Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

** Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

3. Re claim 6, Applicants' convincing remarks (10/05/2005 remarks page 9-10) have overcome rejection in the last office action of claim 6 under 35 U.S.C. 103(a) as being unpatentable over either Kim (2004/0194303) or Applicant's admitted prior art taken with Hirose (6,613,986) (a corrected reference, instead of DiFranco 5,332,486 reference), since the combined references of do not fairly establish a *prima facie* case of obvious of the claimed invention as recited in claim 6.

4. Applicant's remarks filed October 05, 2005 with respect to other pending claims have been considered but they are not persuasive, and moot in view of the new ground(s) of rejection.

5. Applicant mainly remarked that "...step (E) refers to forming circuit patterns on the uppermost and lowermost circuit layers 506b and 506c **only** after the circuit layers and insulating layers are pressed into a circuit board..." (at remark page 6), and that "...the prior art...has circuit patterns formed on the outermost circuit layers before pressing..., the description of the prior art in the specification does not meet the limitations of Claim 1..." (e.g. remark page 7-8).

In response, this is noted and found unconvincing. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

Nowhere in the claims, such as base claim 1, recites the term "...only...". Applicant's prior art anticipatively teaches the claimed invention. As shown in Figures 3-4 and related text of Applicant's prior art, the prior art method comprises alternatively arranging circuit layers and

the insulating layers at predetermined positions (Fig 3), and then pressing to obtain a (D) pressing the arranged circuit and insulating layers (Fig 4; pages 8-9), wherein circuit patterns from the plated copper 105 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 4,1d; page 5, line 21 through page 6). As can be especially seen, "forming circuit patterns..." are performed at the beginning in the sub-step (c) of step (A) of claim 1. Accordingly, Applicant's prior art and Kim clearly teach the claimed subject matter of forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-102

Michael Trinh
Primary Examiner